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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,654	04/02/2004	Shunpei Yamazaki	0756-7279	9416

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EXAMINER	
KARIMY, MOHAMMAD TIMOR	
ART UNIT	PAPER NUMBER
2894	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,654	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	MOHAMMAD Timor KARIMY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48,52,56,61-63 and 66-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48,52,56,61-63 and 66-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Product-by-Process Limitations

1. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; IN re Wethheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 48, 52, 56, 61-63, 66-68 and 70-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (US Patent 5,085,973) in view of Nicholas (US Patent 5,132,821) and Brody et al (US Patent 3,657,613).

Regarding claim 48, Shimizu teaches in figures 1-3 a semiconductor device comprising:

a pair of flexible insulating substrates 1 opposing to each other (Fig. 1);

a thin film transistor 4 formed over the substrate, the thin film transistor having a semiconductor film comprising silicon (inherent, column 2 and line19); and

a layer 3 comprising resin covering the thin film transistor 4 (Fig. 1), wherein the semiconductor device is flexible (due to usage of resinous substrate, the device is flexible).

Shimizu does not disclose a resinous layer formed over one of the pair of the flexible substrate. However, Nicholas and Brody discloses semiconductor devices wherein there is an insulating layer (note Nicholas's SiOx layer 31 in Fig. 2 and Brody's resinous layer 124 in Fig. 1) over one of the flexible substrates. Though Nicolas teaches SiOx for the insulating layer, nonetheless, Brody highlights the benefits of a resinous material due to its characteristics of forming smooth surfaces for subsequent deposition processes. Shimizu, Nicholas and Brody are analogous art (they deal with thin film transistors). At the time of the invention, it would have been apparent to those having ordinary skill in the art to combine said three teachings to include a resinous insulating layer over a flexible substrate for the benefit of having a smooth insulating

layer surface for subsequent formation of device components. As such, Shimizu, Nicholas and Brody are combinable.

Regarding claim 61, Shimizu teaches wherein the silicon is amorphous silicon (column 2 and line 19).

Regarding claim 62, though Shimizu implicitly teaches microcrystalline silicon in the semiconductor film of the TFT (see claim 48); however, if it is determined that Shimizu has not disclosed said claimed dimension (i.e. crystalline silicon), then Nicholas teaches crystalline silicon in a semiconductor layer of a thin film transistor due to crystalline silicon's superior carrier mobility (e.g. column 6 and lines 23).

Regarding claim 66, Shimizu teaches a semiconductor device according to claim 52, wherein the flexible insulating substrate comprises a plastic substrate (column 3 line 41).

Regarding claim 67, Shimizu teaches a semiconductor device according to claim 52, wherein the flexible insulating substrate comprises polyimide (polyimide is a type of resin).

Regarding claim 68, Shimizu and Brody teach a semiconductor device according to claim 52, wherein the resinous layer comprises acrylic resin (Brody's Fig. 1 and note Shimizu's column 7, lines 11-20).

Regarding claim 70, Shimizu teaches a semiconductor device according to claim 52, wherein the thin film transistor comprises an inverted-staggered TFT (Fig. 1).

Regarding claim 71, Shimizu teaches a semiconductor device according to claim 52, wherein the thin film transistor comprises a coplanar TFT (Fig. 1).

Regarding claim 52, Shimizu teaches in figures 1-3 a semiconductor device comprising:

a pair of flexible insulating substrates 1 opposing to each other (Fig. 1);

a thin film transistor (TFT) 4 formed over the resinous layer, the thin film transistor having a semiconductor film comprising silicon (inherent, column 2 and line19); and

a layer 3 comprising resin covering the thin film transistor 4 (Fig. 1), wherein the semiconductor device is flexible (due to usage of resinous substrate, the device is flexible).

Shimizu does not disclose a resinous layer formed over one of the pair of the flexible substrate. However, Nicholas and Brody discloses semiconductor devices wherein there is an insulating layer (note Nicholas's SiOx layer 31 in Fig. 2 and Brody's resinous layer 124 in Fig. 1) over one of the flexible substrates. Though Nicolas teaches SiOx for the insulating layer, nonetheless, Brody highlights the benefits of a resinous material due to its characteristics of forming smooth surfaces for subsequent deposition processes. Shimizu, Nicholas and Brody are analogous art (they deal with thin film transistors). At the time of the invention, it would have been apparent to those having ordinary skill in the art to combine said three teachings to include a resinous insulating layer over a flexible substrate for the benefit of having a smooth insulating layer surface for subsequent formation of device components. As such, Shimizu, Nicholas and Brody are combinable.

Additionally, Shimizu implicitly teaches crystalline silicon in the semiconductor film of the TFT; however, if it is determined that Shimizu has not disclosed said claimed dimension (i.e. crystalline silicon), then Nicholas teaches crystalline silicon (e.g. semiconductor layer 32) in a semiconductor layer of a thin film transistor due to crystalline silicon's superior carrier mobility.

Regarding claim 56, Shimizu teaches in figures 1-3 a semiconductor device comprising:

a pair of flexible insulating substrates 1 opposing to each other (Fig. 1);

a thin film transistor (TFT) 4 formed over the resinous layer, and

a layer 3 comprising resin covering the thin film transistor 4 (Fig. 1), wherein the thin film transistor having a semiconductor film comprising silicon (inherent, column 2 and line19); and

the semiconductor device is flexible (due to usage of resinous substrate, the device is flexible).

Shimizu does not disclose a resinous layer formed over one of the pair of the flexible substrate. However, Nicholas and Brody discloses semiconductor devices wherein there is an insulating layer (note Nicholas's SiOx layer 31 in Fig. 2 and Brody's resinous layer 124 in Fig. 1) over one of the flexible substrates. Though Nicolas teaches SiOx for the insulating layer, nonetheless, Brody highlights the benefits of a resinous material due to its characteristics of forming smooth surfaces for subsequent deposition processes. Shimizu, Nicholas and Brody are analogous art (they deal with

thin film transistors). At the time of the invention, it would have been apparent to those having ordinary skill in the art to combine said three teachings to include a resinous insulating layer over a flexible substrate for the benefit of having a smooth insulating layer surface for subsequent formation of device components. As such, Shimizu, Nicholas and Brody are combinable.

Additionally, Shimizu implicitly teaches crystalline silicon in the semiconductor film of the TFT; however, if it is determined that Shimizu has not disclosed said claimed dimension (i.e. crystalline silicon), then Nicholas teaches crystalline silicon (e.g. semiconductor layer 32) in a semiconductor layer of a thin film transistor due to crystalline silicon's superior carrier mobility.

Also, it is important to note that the limitation "**wherein the crystalline silicon is formed by a laser irradiation**" is a product by process limitation and it does not structurally distinguish over the prior art.

Regarding claim 63, the limitation "**wherein the laser irradiation is conducted by using at least one selected from the group consisting of KrF excimer laser and XeCl laser**" is a product by process limitation and it does not result to a structurally distinguishable product over the prior art.

4. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu, Brody and Nicholas as applied to claim 52 above, and in further view of Takenouchi et al. (US Patent 5,427,961).

In regards to claim 69, Shimizu, Brody and Nicholas do not disclose the following:

a) the resinous layer comprises at least one selected from the group consisting of methyl esters of acrylic acid, ethyl esters of acrylic acid, butyl esters of acrylic acid, and 2-ethylhexyl esters of acrylic acid.

However, Takenouchi et al. ("Takenouchi") discloses a resinous layer that comprises at least one selected from the group consisting of methyl esters of acrylic acid, ethyl esters of acrylic acid, butyl esters of acrylic acid, and 2-ethylhexyl esters of acrylic acid (For Example: See Column 3 Lines 55-59). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device to include a resinous layer that comprises at least one selected from the group consisting of methyl esters of acrylic acid, ethyl esters of acrylic acid, butyl esters of acrylic acid, and 2-ethylhexyl esters of acrylic acid as disclosed in Takenouchi because it aids in preventing wear (For Example: See Column 4 Lines 47-50). Additionally, since Shimizu, Brody, Nicholas and Takenouchi are from the same field of endeavor, the purpose disclosed by Takenouchi would have been recognized in the pertinent art.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD Timor KARIMY whose telephone number is (571) 272-9006. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

mtk

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894